ABSTRACT OF THE DISCLOSURE

A wafer-level package includes a semiconductor wafer having at least one semiconductor chip circuit forming region each including a semiconductor chip circuit each provided with test chip terminals and non test chip terminals, at least one external connection terminal, at least one redistribution trace provided on the semiconductor wafer, at least one testing member, and an insulating material. A first end of the redistribution trace is connected to one of the test chip terminals and a second end of said redistribution trace is extended out to a position offset from the chip terminals. The testing member is provided in an outer region of the semiconductor chip circuit forming region, and the second end of the redistribution trace is connected to the testing member.